M16C/80, M32C/83 Group

Differences between M16C/80 and M32C/83

1. Abstract

This issue is the reference matelials ot function differences between M16C/80 and M32C/83.

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M16C/80, M32C/83 Group

3. Contents

3.1 Function Differences

Table 3.1.1 and table 3.1.2 show the Function Differences.

Table 3.1.1 Function Differences (1) (Note1)

Item	M16C/80	M32C/83
Basic Instructions	106 instructions	108 instructions (Add SHANC, SHLNC instructions)
Shortest Instruction Execution Time	50ns(f(X_{IN})=20MHz)	31.3ns(f(BCLK)=32MHz)
Supply Voltage	4.2V to 5.5V(f(X_{IN})=20MHz) 2.7V to 5.5V(f(X_{IN})=10MHz)	4.2V to 5.5V (f(BCLK)=32MHz, through VDC) 3.0V to 5.5V (f(BCLK)=20MHz, through VDC) 3.0V to 3.6V (f(BCLK)=20MHz, not through VDC)
Clock Generating Circuit	X_{IN}, X_{CIN}	X_{IN}, X_{CIN}, PLL, On-chip oscillator
Main clock, sub clock drive capability select function	Have	None
Peripheral Function clock	f_1, f_8, f_{32}, f_{C32}	f_1, f_8, f_{C32}, f_{2n} (n=0 ot 15. No division when n=0)
Oscillation Stop Detect Function	None	Have
Power Consumption	45mA(5V, f(X_{IN})=20MHz)	41mA (VCC=5V, f(BCLK)=32MHz) 38mA (VCC=5V, f(BCLK)=30MHz) 26mA (VCC=3.3V, f(BCLK)=20MHz) 470μA (VCC=5V, f(XCIN)=32kHz, in wait mode) 340μA (VCC=3.3V, f(XCIN)=32kHz, through VDC in wait mode 5.0μA (VCC=3.3V, f(XCIN)=32kHz, not through VDC in wait mode) 0.4μA (VCC=5V, in stop mode) 0.4μA (VCC=3.3V, in stop mode)
Access to SFR	1 wait fixed	Variable (1 to 2 waits)
Protect	Can be set for PM0, PM1, CM0, CM1, MCD, PD9, PS3 register	Can be set for PM0, PM1, CM0, CM1, MCD, PD9, PS3, CM2, PLC0, PLC1, INVC0, INVC1, PLV, VDC0 register
DMA Request Factors	Falling edge or both edges of input signals to the $\overline{INT0}$ to $\overline{INT3}$ pin Timer A0 to timer A4 interrupt requests Timer B0 to timer B5 interrupt requests UART0 to UART4 transmit and receive interrupt requests A/D conversion interrupt request Software trigger	The next interrupt is added to M16C/80. A/D1 conversion interrupt request Intelligent I/O interrupt request CAN interrupt request
DMAII Function	None	Have
Timer A, Timer B Count Source	Selectable: f_1, f_8, f_{32}, f_{C32}	Selectable: f_1, f_8, f_{C32}, f_{2n}(n=0 to 15,.No division when n=0)

Note 1: About the details and the characteristics, refer to hardware manual.

Table 3.1.2 Function Differences (2) (Note1)

Item	M16C/80	M32C/83
Three-Phase Motor Control Timer Dead Time	Have	Selectable
Three-Phase Motor Control Timer Dead Time Trigger	Fixed	Selectable
Three-Phase Motor Control Timer Count Source	Selectable: f_1, f_8, f_{32}, fc_{32}	Selectable: f_1, f_8, fc_{32}, f_{2n} (n=0 to 15. No division when n=0)
Serial I/O	(Clock synchronous serial I/O, Clock asynchronous serial I/O) × 2 (Clock synchronous serial I/O, Clock asynchronous serial I/O , I²C bus™ (Note 2), IEBus™(Note 3), SIM interface) × 3	(Clock synchronous serial I/O, Clock asynchronous serial I/O, I²C bus™ (Note 2), IEBus™(Note 3), GCI bus, SIM interface) × 5
Serial I/O $\overline{CTS}/\overline{RTS}$ Separate Function	Can be used in UART0	None
Serial I/O Transfer Clock Output from Multiple Pins	Can be used in UART1	None
Serial I/O TxD, RxD I/O Polarity Switching Function	Can be used in UART2 to UART4	Can be used in UART0 to UART4
Serial I/O Sleep Function	Can be used in UART0, UART1	None
Serial I/O Count Source	Selectable: f_1, f_8, f_{32}	f_1, f_8, f_{2n}(n=0 to 15. No division when n=0)
Serial I/O Overrun error occur timing	This error occurs when the next data is ready before contents of UiRB register (i=0 to 4) are read out	This error occurs if the serial I/O started receiving the next data before reading the UiRB register (i=0 to 4) and received the 7th bit of the next data (Clock synchronous serial I/O). This error occurs if the serial I/O started receiving the next data before reading the UiRB register and received the bit one before the last stop bit of the next data (Clock asynchronous serial I/O).
Serial I/O $\overline{RTS}$ Timing	Assert low when reception is completed	Assert low when receive buffer is read
Serial I/O I²C Mode	Start condition, stop condition: Not auto-generation	Start condition, stop condition: Auto-generation
Serial I/O I²C mode SDA delay	SDA digital delay count source: 1/f(XIN)	SDA digital delay count source: BRG
CAN Module	None	1 channel
Intelligent I/O	None	4 group
A/D Converter	1 circuit, 10 channels	2 circuits, 34 channels
A/D Converter Maximum Operating Frequency	10MHz	16MHz (VCC=5.0V)
A/D Converter Operating Clock	Selectable: f_{AD}, $f_{AD}/2$, $f_{AD}/4$	Selectable: f_{AD}, $f_{AD}/2$, $f_{AD}/3$, $f_{AD}/4$

Note 1: About the details and the characteristics, refer to hardware manual.
Note 2: I²C bus is a trademark of Koninklijke Philips Electronics N. V.
Note 3: IEBus is a trademark of NEC Electronics Corporation.

3.2 Pin function Differences

Table 3.2.1 and table 3.2.2 show the Pin Function Differences.

Table 3.2.1 Pin Function Differences (1/2)

M16C/80	M32C/83	Remarks
P9$_2$/TB2$_{IN}$/TxD3/SDA3/SRxD3	P9$_2$/TB2$_{IN}$/TxD3/SDA3/SRxD3/IE$_{OUT}$/ISTxD2/OUTC2$_0$	Add IE$_{OUT}$/ISTxD2/OUTC2$_0$
P9$_1$/TB1$_{IN}$/RxD3/SCL3/STxD3	P9$_1$/TB1$_{IN}$/RxD3/SCL3/STxD3/ISRxD2/IE$_{IN}$	Add ISRxD2/IE$_{IN}$
P14$_3$	P14$_3$/INPC1$_7$/OUTC1$_7$	Add INPC1$_7$/OUTC1$_7$
P14$_2$	P14$_2$/INPC1$_6$/OUTC1$_6$	Add INPC1$_6$/OUTC1$_6$
P14$_1$	P14$_1$/OUTC1$_5$	Add OUTC1$_5$
P14$_0$	P14$_0$/OUTC1$_4$	Add OUTC1$_4$
P8$_7$/X$_{CIN}$	P8$_7$/X$_{CIN}$/V$_{CONT}$	Add V$_{CONT}$
P8$_3$/$\overline{INT1}$	P8$_3$/$\overline{INT1}$/CAN$_{IN}$	Add CAN$_{IN}$
P8$_2$/INT0	P8$_2$/INT0/OUTC3$_2$/CAN$_{OUT}$/ISRxD3	Add OUTC3$_2$/CAN$_{OUT}$/ISRxD3
P8$_1$/TA4$_{IN}$/$\overline{U}$	P8$_1$/TA4$_{IN}$/$\overline{U}$/OUTC3$_0$/ISTxD3	Add OUTC3$_0$/ISTxD3
P8$_0$/TA4$_{OUT}$/U	P8$_0$/TA4$_{OUT}$/U/INPC0$_2$/ISRxD0/BE0$_{IN}$	Add INPC0$_2$/ISRxD0/BE0$_{IN}$
P7$_7$/TA3$_{IN}$	P7$_7$/TA3$_{IN}$/INPC0$_1$/OUTC0$_1$/ISCLK0/CAN$_{IN}$	Add INPC0$_1$/OUTC0$_1$/ISCLK0/CAN$_{IN}$
P7$_6$/TA3$_{OUT}$	P7$_6$/TA3$_{OUT}$/INPC0$_0$/OUTC0$_0$/ISTxD0/BE0$_{OUT}$/CAN$_{OUT}$	Add INPC0$_0$/OUTC0$_0$/ISTxD0/BE0$_{OUT}$/CAN$_{OUT}$
P7$_5$/TA2$_{IN}$/$\overline{W}$	P7$_5$/TA2$_{IN}$/$\overline{W}$/INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$	Add INPC1$_2$/OUTC1$_2$/ISRxD1/BE1$_{IN}$
P7$_4$/TA2$_{OUT}$/W	P7$_4$/TA2$_{OUT}$/W/INPC1$_1$/OUTC1$_1$/ISCLK1	Add INPC1$_1$/OUTC1$_1$/ISCLK1
P7$_3$/V/$\overline{CTS2}$/$\overline{RTS2}$/TA1$_{IN}$	P7$_3$/V/$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$/TA1$_{IN}$/OUTC1$_0$/ISTxD1/BE1$_{OUT}$	Add OUTC1$_0$/ISTxD1/BE1$_{OUT}$/$\overline{SS2}$
P7$_1$/RxD2/SCL2/TA1$_{OUT}$/TB5$_{IN}$	P7$_1$/RxD2/SCL2/TA1$_{OUT}$/TB5$_{IN}$/STxD2/OUTPC2$_2$/ISRxD2/IE$_{IN}$	Add STxD2/OUTPC2$_2$/ISRxD2/IE$_{IN}$
P7$_0$/TxD2/SDA2/TA0$_{OUT}$	P7$_0$/TxD2/SDA2/TA0$_{OUT}$/SRxD2/OUTC2$_0$/ISTxD2/IE$_{OUT}$	Add SRxD2/OUTC2$_0$/ISTxD2/IE$_{OUT}$
P6$_7$/TxD1	P6$_7$/TxD1/SDA1/SRxD1	Add SDA1/SRxD1
P6$_6$/RxD1	P6$_6$/RxD1/SCL1/STxD1	Add SCL1/STxD1
P6$_4$/$\overline{CTS1}$/$\overline{RTS1}$/$\overline{CTS0}$/CLKS1	P6$_4$/$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$/OUTC2$_1$/ISCLK2	Add $\overline{SS1}$/OUTC2$_1$/ISCLK2 Delete $\overline{CTS0}$/CLKS1
P6$_3$/TxD0	P6$_3$/TxD0/SDA0/SRxD0	Add SDA0/SRxD0
P6$_2$/RxD0	P6$_2$/RxD0/SCL0/STxD0	Add SCL0/STxD0
P6$_0$/$\overline{CTS0}$/$\overline{RTS0}$	P6$_0$/$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$	Add $\overline{SS0}$
P13$_7$	P13$_7$/OUTC2$_7$	Add OUTC2$_7$
P13$_6$	P13$_6$/OUTC2$_1$/ISCLK2	Add OUTC2$_1$/ISCLK2
P13$_5$	P13$_5$/OUTC2$_2$/ISRxD2/IE$_{IN}$	Add OUTC2$_2$/ISRxD2/IE$_{IN}$
P13$_4$	P13$_4$/OUTC2$_0$/ISTxD2/IE$_{OUT}$	Add OUTC2$_0$/ISTxD2/IE$_{OUT}$
P13$_3$	P13$_3$/OUTC2$_3$	Add OUTC2$_3$
P13$_2$	P13$_2$/OUTC2$_6$	Add OUTC2$_6$
P13$_1$	P13$_1$/OUTC2$_5$	Add OUTC2$_5$
P13$_0$	P13$_0$/OUTC2$_4$	Add OUTC2$_4$
P12$_7$	P12$_7$/OUTC3$_7$	Add OUTC3$_7$
P12$_6$	P12$_6$/OUTC3$_6$	Add OUTC3$_6$
P12$_5$	P12$_5$/OUTC3$_5$	Add OUTC3$_5$
P12$_4$	P12$_4$/OUTC3$_4$	Add OUTC3$_4$
P12$_3$	P12$_3$/OUTC3$_3$	Add OUTC3$_3$
P12$_2$	P12$_2$/OUTC3$_2$/ISRxD3	Add OUTC3$_2$/ISRxD3
P12$_1$	P12$_1$/OUTC3$_1$/ISCLK3	Add OUTC3$_1$/ISCLK3
P12$_0$	P12$_0$/OUTC3$_0$/ISTxD3	Add OUTC3$_0$/ISTxD3

Table 3.2.2 Pin Function Differences (2/2)

M16C/80	M32C/83	Remarks
P2$_7$/A$_7$(/D$_7$)	P2$_7$/A$_7$(/D$_7$)/AN2$_7$	Add AN2$_7$
P2$_6$/A$_6$(/D$_6$)	P2$_6$/A$_6$(/D$_6$)/AN2$_6$	Add AN2$_6$
P2$_5$/A$_5$(/D$_5$)	P2$_5$/A$_5$(/D$_5$)/AN2$_5$	Add AN2$_5$
P2$_4$/A$_4$(/D$_4$)	P2$_4$/A$_4$(/D$_4$)/AN2$_4$	Add AN2$_4$
P2$_3$/A$_3$(/D$_3$)	P2$_3$/A$_3$(/D$_3$)/AN2$_3$	Add AN2$_3$
P2$_2$/A$_2$(/D$_2$)	P2$_2$/A$_2$(/D$_2$)/AN2$_2$	Add AN2$_2$
P2$_1$/A$_1$(/D$_1$)	P2$_1$/A$_1$(/D$_1$)/AN2$_1$	Add AN2$_1$
P2$_0$/A$_0$(/D$_0$)	P2$_0$/A$_0$(/D$_0$)/AN2$_0$	Add AN2$_0$
P0$_7$/D$_7$	P0$_7$/AN0$_7$/D$_7$	Add AN0$_7$
P0$_6$/D$_6$	P0$_6$/AN0$_6$/D$_6$	Add AN0$_6$
P0$_5$/D$_5$	P0$_5$/AN0$_5$/D$_5$	Add AN0$_5$
P0$_4$/D$_4$	P0$_4$/AN0$_4$/D$_4$	Add AN0$_4$
P11$_3$	P11$_3$/OUTC1$_3$	Add OUTC1$_3$
P11$_2$	P11$_2$/OUTC1$_2$/INPC1$_2$/ISRxD1/BE1$_{IN}$	Add OUTC1$_2$/INPC1$_2$/ISRxD1/BE1$_{IN}$
P11$_1$	P11$_1$/OUTC1$_1$/INPC1$_1$/ISCLK1	Add OUTC1$_1$/INPC1$_1$/ISCLK1
P11$_0$	P11$_0$/OUTC1$_0$/ISTxD1/BE1$_{OUT}$	Add OUTC1$_0$/ISTxD1/BE1$_{OUT}$
P0$_3$/D$_3$	P0$_3$/AN0$_3$/D$_3$	Add AN0$_3$
P0$_2$/D$_2$	P0$_2$/AN0$_2$/D$_2$	Add AN0$_2$
P0$_1$/D$_1$	P0$_1$/AN0$_1$/D$_1$	Add AN0$_1$
P0$_0$/D$_0$	P0$_0$/AN0$_0$/D$_0$	Add AN0$_0$
P15$_7$	P15$_7$/AN15$_7$/INPC0$_7$	Add AN15$_7$/INPC0$_7$
P15$_6$	P15$_6$/AN15$_6$/INPC0$_6$	Add AN15$_6$/INPC0$_6$
P15$_5$	P15$_5$/AN15$_5$/INPC0$_5$/OUTC0$_5$	Add AN15$_5$/INPC0$_5$/OUTC0$_5$
P15$_4$	P15$_4$/AN15$_4$/INPC0$_4$/OUTC0$_4$	Add AN15$_4$/INPC0$_4$/OUTC0$_4$
P15$_3$	P15$_3$/AN15$_3$/INPC0$_3$	Add AN15$_3$/INPC0$_3$
P15$_2$	P15$_2$/AN15$_2$/INPC0$_2$/ISRxD0/BE0$_{IN}$	Add AN15$_2$/INPC0$_2$/ISRxD0/BE0$_{IN}$
P15$_1$	P15$_1$/AN15$_1$/INPC0$_1$/OUTC0$_1$/ISCLK0	Add AN15$_1$/INPC0$_1$/OUTC0$_1$/ISCLK0
P15$_0$	P15$_0$/AN15$_0$/INPC0$_0$/OUTC0$_0$/ISTxD0/BE0$_{OUT}$	Add AN15$_0$/INPC0$_0$/OUTC0$_0$/ISTxD0/BE0$_{OUT}$

3.3 SFR Differences

Table 3.3.1 and table 3.2.3 show the SFR Differences.

Table 3.3.1 SFR Differences (1/3)

M16C/80	M32C/83	Remarks
PM1	PM1	Add bit 3. Change set value of reserved bit.
CM0	CM0	Change function
CM1	CM1	Add bit 7. Change function.
PRCR	PRCR	Add bit 3. Change function.
-	CM2	
-	PLV	
-	VDC0	
-	VDC1	
BCN3IC	BCN0IC/BCN3IC	Shard with BCN0IC register
ADIC	AD0IC	Change register name
-	AD1IC	
BCN4IC	BCN1IC/BCN4IC	Shard with BCN1IC register
RLVL	RLVL	Add bit 5
-	Intelligent I/O, CAN related interrupt control register	
-	Intelligent I/O interrupt request register	
-	Intelligent I/O interrupt enable register	
-	Intelligent I/O, related register	
-	IPS	
-	AD1 related register	
-	CAN related register	
-	U4SMR4	
U4SMR2	U4SMR2	Change function
U4SMR	U4SMR	Add bit 7
U4C0	U4C0	Change function
U4C1	U4C1	Change function
INVC1	INVC1	Add bits 5, 6
IFSR	IFSR	Add bits 6, 7
-	U3SMR4	
U3SMR2	U3SMR2	Change function
U3SMR	U3SMR	Add bit 7
U3C1	U3C1	Change function
-	U2SMR4	
U2SMR3	U2SMR3	Add bits 0 to 4
U2SMR2	U2SMR2	Change function
U2SMR	U2SMR	Add bit 7
U2C1	U2C1	Change function
-	TB2SC	
-	TCSPR	

Table 3.3.2 SFR Differences (2/3)

M16C/80	M32C/83	Remarks
-	U0SMR4	
-	U0SMR3	
-	U0SMR2	
-	U0SMR1	
-	U0SMR	
U0MR	U0MR	Address change from 0360h to 0368h. Change function.
U0BRG	U0BRG	Address change from 0361h to 0369h.
U0TB	U0TB	Address change from 0363h-0362h to 036Bh-036Ah.
U0C0	U0C0	Address change from 0364h to 036Ch
U0C1	U0C1	Address change from 0365h to 036Dh. Add bits 4 to 7.
U0RB	U0RB	Address change from 0367h-0366h to 036Bh-036Ah
-	U1SMR3	
-	U1SMR2	
-	U1SMR	
U1MR	U1MR	Address change from 0368h to 02E8h. Change function.
U1BRG	U1BRG	Address change from 0369h to 02E9h.
U1TB	U1TB	Address change from 036Bh-036Ah to 02EBh-02EAh
U1C0	U1C0	Address change from 036Ch to 02ECh
U1C1	U1C1	Address change from 036Dh to 02EDh. Add bits 4 to 7.
U1RB	U1RB	Address change from 036Fh-036Eh to 02EFh-02EEh
UCON	-	
FMR1	-	
FMR0	FMR0	Address change from 0377h to 0057h
-	PLC0	
-	PLC1	
DM0SL	DM0SL	Change function
DM1SL	DM1SL	Change function
DM2SL	DM2SL	Change function
DM3SL	DM3SL	Change function
AD0	AD00	Change register name
AD1	AD01	Change register name
AD2	AD02	Change register name
AD3	AD03	Change register name
AD4	AD04	Change register name
AD5	AD05	Change register name
AD6	AD06	Change register name
AD7	AD07	Change register name
ADCON2	AD0CON2	Change register name. Add bits 4 to 7.
ADCON0	AD0CON0	Change register name. Change function.
ADCON1	AD0CON1	Change register name. Change function.

Table 3.3.3 SFR Differences (3/3)

M16C/80	M32C/83	Remarks
-	PS8	
-	PS9	
PSC	PSC	Add bits 1 to 4, 6. Change function.
PS0	PS0	Add bits 2, 6. Change function.
PS1	PS1	Add bit 7. Change function.
PSL0	PSL0	Add bits 1, 6. Change function.
PSL1	PSL1	Add bits 1, 5, 6. Change function.
PS2	PS2	Add bit 2. Change function.
PS3	PS3	Change function
PSL2	PSL2	Add bits 1, 2.
PSL3	PSL3	Add bit 2
-	PS5	
-	PS6	
-	PS7	

3.4 Interrupt Vector Differences

Table 3.4.1 shows the Fixed Vector Table Differences. Table 3.4.2 shows the Relocatable Vector Table Differences.

Table 3.4.1 Fixed Vector Table Differences

M16C/80 Interrupt Factor	M32C/83 Interrupt Factor	Remarks
Watchdog Timer	Watchdog Timer Oscillation Stop Detection	Add Watchdog Timer

Table 3.4.2 Relocatable Vector Table Differences

M16C/80 Interrupt Factor	M32C/83 Interrupt Factor	Software Interrupt Number
-	A/D1	7
UART0 transmission	UART0 transmission, NACK	17
UART0 reception	UART0 reception, ACK	18
UART1 transmission	UART1 transmission, NACK	19
UART1 reception	UART1 reception, ACK	20
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect (UART2)	Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, Fault Error (UART2)	39
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, Fault Error (UART3)	Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, Fault Error (UART3 or UART0)	40
Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, Fault Error (UART4)	Bus Conflict Detect, Start Condition Detect, Stop Condition Detect, Fault Error (UART4 or UART1)	41
-	Intelligent I/O Interrupt 0	44
-	Intelligent I/O Interrupt 1	45
-	Intelligent I/O Interrupt 2	46
-	Intelligent I/O Interrupt 3	47
-	Intelligent I/O Interrupt 4	48
-	Intelligent I/O Interrupt 5	49
-	Intelligent I/O Interrupt 6	50
-	Intelligent I/O Interrupt 7	51
-	Intelligent I/O Interrupt 8	52
-	Intelligent I/O Interrupt 9, CAN0	53
-	Intelligent I/O Interrupt 10, CAN1	54
-	Intelligent I/O Interrupt 11, CAN2	57

3.5 Support Tool Differences

Table 3.5.1 shows the support tool differences.

Table 3.5.1 Support Tool Differences

Tool information	M16C/80 Tool Product	M32C/83 Tool Product (Max.20MHz)	M32C/83 Tool Product (Max.30MHz)
C Compiler	M3T-NC308WA	M3T-NC308WA	M3T-NC308WA
Real-time OS	M3T-MR308	M3T-MR308	M3T-MR308
Simulator Debugger	M3T-PD308SIM	M3T-PD308SIM	M3T-PD308SIM
Emulator Debugger	M3T-PD308	M3T-PD3083	M3T-PD308F
Emulator	PC4701U	PC4701U	PC7501
Emulation Pod, Emulation Probe	M30803T-RPD-E	M30830T-RPD-E	M30830T-EPB

4. Reference

Renesas Technology Corporation Home Page

http://www.renesas.com/

E-mail Support

E-mail: csc@renesas.com

Hardware Manual

M32C/83 Group Hardware Manual
(Use the latest version on the home page: http://www.renesas.com)

User's Manual

M16C/80 Group User's Manual
(Use the latest version on the home page: http://www.renesas.com)

REVISION HISTORY

Rev.	Date	Description	
		Page	Summary
1.01	2005.01.12	-	First edition issued
1.02	2005.04.15	2	Add A/D converter maximum operating frequency

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